STORED PROGRAM CONTROL (SPC) EXCHANGE

In the strowger's step by step switching system and crossbar switching system,electromechanical components were used for both switching andcontrol elements. In 1965, Bell system installed the first computer controlled switching systemwhich uses a stored program digital computer for its control functions. The SPC conceptspermits the features like abbreviated dialing, call forwarding, call waiting etc. The SPC providessignificant advantages to end users. The SPC enables easier number changes, automated calltracing message unit accounting (for billing) etc.

Basic of SPC

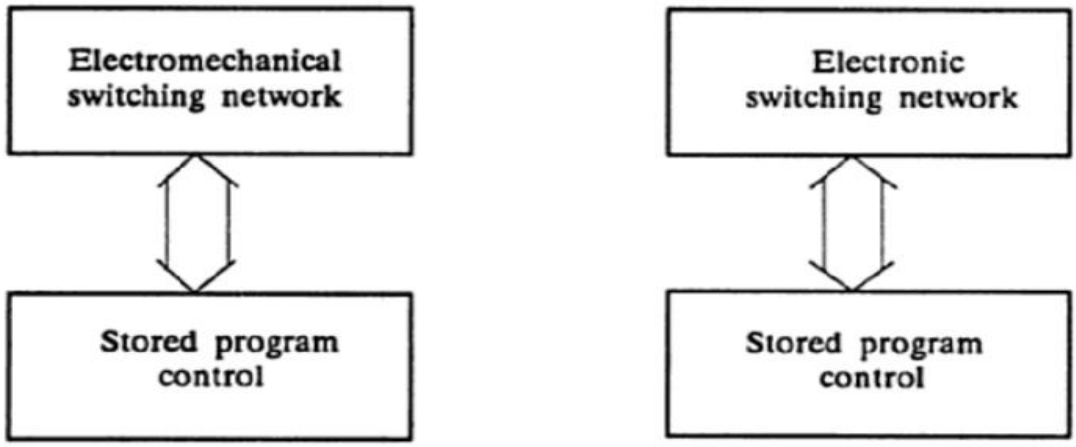
Two types of SPC switching system

(1)Electro-mechanicalSwitching

SPC+Electro-mechanical switching network

(2)ElectronicSwitching

SPC+Electronic switching network



STORED PROGRAM CONTROL (SPC) EXCHANGE

Fig.3 Electronic space division switching system [1]

Organization of SPC:

CENTRALIZED SPC

It finds broadly application in early SPC switching systems.

DISTRIBUTED SPC

It is Gaining popularity in modern switching systems.

Early electronic switching systems are centralized SPC exchanges and used a single processor to perform the exchange functions. Presently centralized exchanges uses dual processor for high reliability.

Concept

„All the control equipment is replaced by a single powerful processor.

†Configuration of centralized SPC

„Typical organization

„Redundant configuration

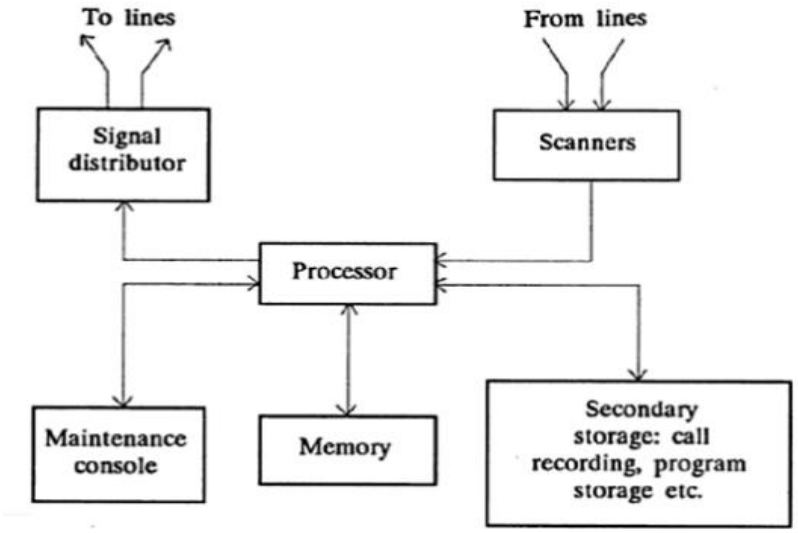


Fig. 3 (a) Centralized SPC organization [1]

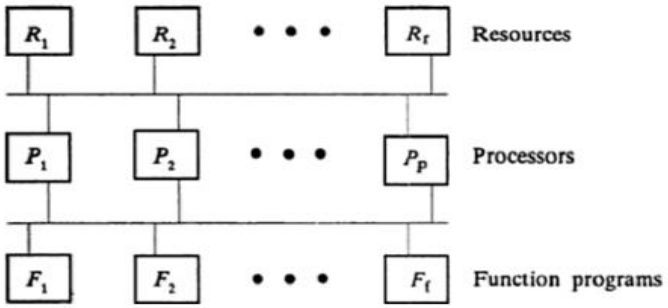


Fig. 3 (b): A redundant Centralized SPC control structure [1]

Operation modes in redundant configuration (e.g. dual processor)

- **Standby mode**
- **„Synchronous duplex mode**
- **„Load sharing mode**
- **Standby mode**

How does it work?

In this mode, any one of the processors will be active and the rest is standby. The standby processor is brought online only when the active processor fail. This mode of exchange uses a secondary storage common to both processors. The active processor copies the status of the system periodically and stores in axis secondary storage. In this mode the processors are not

connected directly. In secondary storage, programs and instructions related to the control functions, routine programs and other required information are stored.

„All processors have the same capability to control the switching procedure.

„One processor is active and the other is on standby, both hardware and software wise.

„The standby processor is brought online only when the active processor fails.

How does the standby processor take over the control properly?

„State of the exchange system should be clear to the standby processor as its starting point.

Which of the subscribers are busy or free?

Which of the trunks are busy or free?

Which of the paths are connected through the switching network?

Reconstitution of the state

Scanning:

- ✓ **The standby processor scans all status signals as soon as it is brought into operation.**
- ✓ **Only the calls which are being established at the time of failure are disturbed.**
- ✓ **Only feasible for small exchanges.**
- ✓ **Shared secondary storage: popular.**

Shared secondary storage:

- ✓ **The active processor copies system status into a secondary storage periodically, say every 5 seconds.**
- ✓ **As soon as a switchover occurs, the online processor loads the most recent update of the system status from the secondary storage and continues the operations.**
- ✓ **Only the calls which changed status between the last update and the failure are disturbed.**
- ✓ **Feasible for large exchanges.**

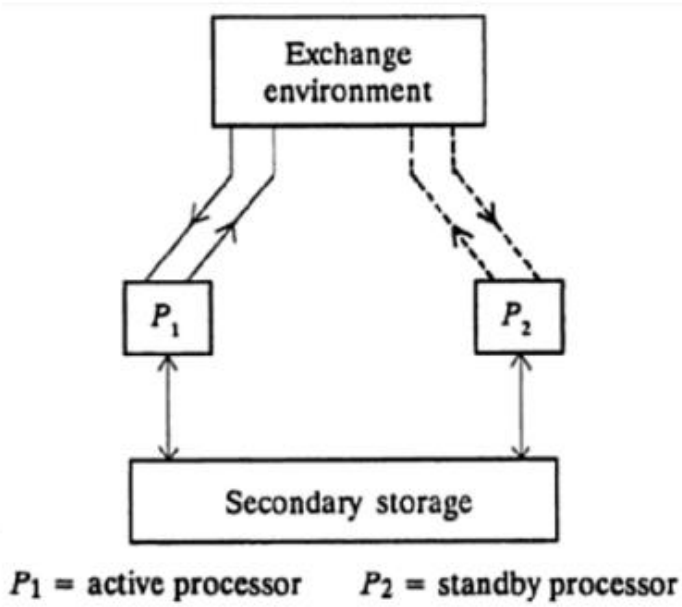


Fig. 3 (c): Standby dual processor configuration [1]

Synchronous duplex mode

How does it work?

In this mode, the processors *p*1 and *p*2 are connected together to exchange instructions and controls. Instead of a secondary storage common to P1 and P2, separate memory M1 and M2 are used. These processors are coupled to exchange stored data. This mode of operation also uses a comparator in between *p*1 and *p*2. The comparator compares the result of the processors.

During normal operation, both processor receives all the information from the exchange and receives related data from their memories. Although only one processor actually controls the exchange and remaining is in synchronism with first one. If a mismatch occurs, the fault is identified by the comparator, and the faulty processor is identified by operating both individually. After the rectification of fault, the processor is brought into service.

- ✓ Both two processors execute the same set of instructions.
- ✓ One of the processor actually controls the exchange.
- ✓ The results from two processors are compared continuously by a comparator.
- ✓ If the results match, the system works normally. Otherwise, a fault occurs, a check-out program is run independently in both two processors to determine which one is faulty.
- ✓ The faulty processor is taken out of service, and the other one works independently.

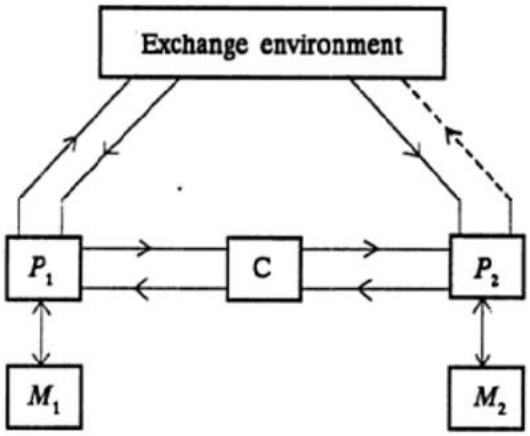


Fig. 3 (d): Synchronous duplex operation [1]

Synchronous duplex mode

- ✓ In case of transient failure of comparator, there are three possibilities exist:
- ✓ Continue with both processors.
- ✓ Take out the active processor and continue with other processor.
- ✓ „Continue with the active processor but remove the other processor from service.

Load sharing mode

How does it work?

- ✓ „ Both two processors have access to entire exchange environment. Each of them has independent memories for redundancy purpose.
- ✓ „ Both two processors are active simultaneously and share the load and the resources dynamically.
- ✓ „ An incoming call is assigned randomly or in a predefined order to one of the processors which then handles the call right through completion.
- ✓ „ Inter-processor links are configured for processors to exchange information needed for mutual coordination and verifying the 'state of health' of the other.

If a processor fails, the other processor takes over the entire load including the calls already set up by the failing processor.

Exclusion mechanism in resource sharing

- ✓ „The processors should not seek the same resource at the same time.
- ✓ „Implementation: hardware & software.

In this mode, the comparator is removed and alternatively an exclusion device (ED) is used. The processors call for ED to share the resources, so that both the processors do not seek the same resource at the same time. In this mode, both the processor are active simultaneously and share the resources of exchange and the load dynamically. If one processor fails, with the

help of ED, the other processor takes over the entire load of the exchange. Under normal operation, each processor handles one half of the calls on a statistical basis. However the exchange operator can vary the processor load for maintenance purpose.

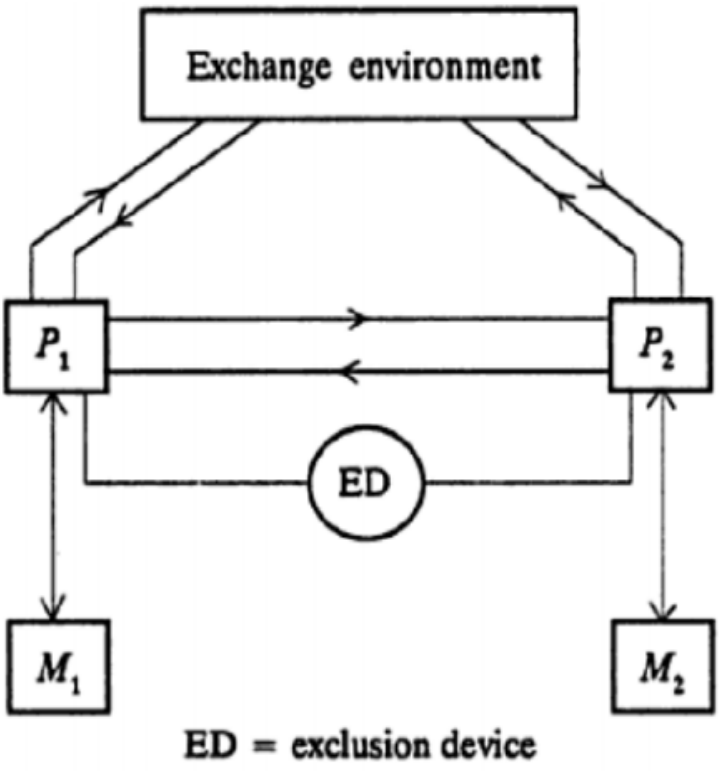


Fig. 3 (e): Load sharing configuration.[1]

Traffic distribution between processors

Load sharing increases the effective traffic capacity by 30 percent compared with synchronous duplex.

Single processor. Availability $A = \frac{MTBF}{MTBF + MTTR}$ ...(4.4)

where MTBF = Mean time between failures

MTTR = Mean time to repair

Unavailability = 1 – A

$$U = 1 - \frac{MTBF}{MTBF + MTTR} \; ; U = \frac{MTTR}{MTBF + MTTR} \quad ...(4.5)$$

If MTBF >> MTTR, $U = \frac{MTTR}{MTBF}$ ...(4.6)

Dual Processor. A dual processor system is said to have failed only when both processor fails and the total system is unavailable. The MTBF of dual processor is given by

$$(MTBF)_D = \frac{(MTBF)^2}{2MTTR} \quad ...(4.7)$$

where $(MTBF)_D$ = MTBF of dual processor

MTBF = MTBF single processor

Availability $$A_D = \frac{(MTBF)_D}{MTTR + (MTBF)_D}$$

Substituting $(MTBF)_D$ in the above equation, we have

$$A_D = \frac{(MTBF)^2 / 2MTTR}{MTTR + \frac{(MTBF)^2}{2MTTR}}$$

$$A_D = \frac{(MTBF)^2}{(MTBF)^2 + 2(MTTR)^2}$$

Unavailability $$U = 1 - A_D = 1 - \frac{(MTBF)^2}{(MTBF)^2 + 2(MTTR)^2}$$

$$= \frac{2(MTTR)^2}{(MTBF)^2 + 2(MTTR)^2}$$

If MTBF >> MTTR, $$U_D = \frac{2(MTTR)^2}{(MTBF)^2}$$

Distributed SPC

The introduction of distributed SPC enabled customers to be provided with a wider range of services than those available with centralized and electromechanical switching system. Instead of all processing being performed by a one or two processor in centralized switching, functions are delegated to separate small processors (referred as regional processors). But central processors are still required to direct the regional processors and to perform more complex tasks. The distributed SPC offers better availability and reliability than the centralized SPC. Entire exchange control functions may be decomposed either horizontally or vertically for distributed processing. In vertical decomposition, the exchange environment is divided into several blocks and each block is assigned to a processor that performs all control functions related to that block of equipment. In horizontal decomposition, each processor performs one or some of the exchange control functions. Figure shows the distributed control where switching equipment is divided into parts, each of which has its own processor.

CONCEPT OF DISTRIBUTED SPC

The control functions are shared by many processors within the exchanges.

- ✓ ***Background***
- ✓ **Low cost processors**

Advantages

- Better Availability
- Better Reliability

Decomposition of Control Functions

- **Vertical decomposition**

The exchange environment is divided into several blocks.

Each block is assigned to a processor.

A processor performs all control functions related to the corresponding block.

The processor in each block may be duplicated for redundancy purposes.

Obviously, the control system consists of a number of control units.

The modular structure is flexible for system expanding.

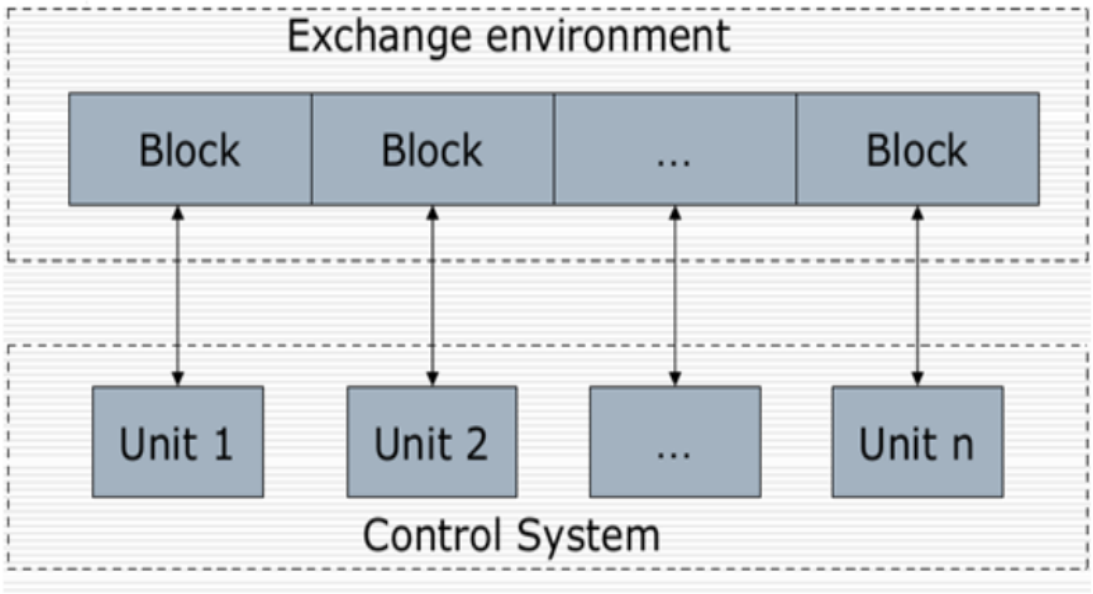


Fig. 3 (f): Vertical decomposition[1]

- **Horizontal decomposition**

✓ The control functions are divided into groups, e.g. event monitoring, call processing, and O&M functions.

✓ Each processor performs only one or some of the exchange control functions.

✓ A chain of processors are used to perform the entire control of the exchange.

✓ The entire chain may be duplicated to provide redundancy.

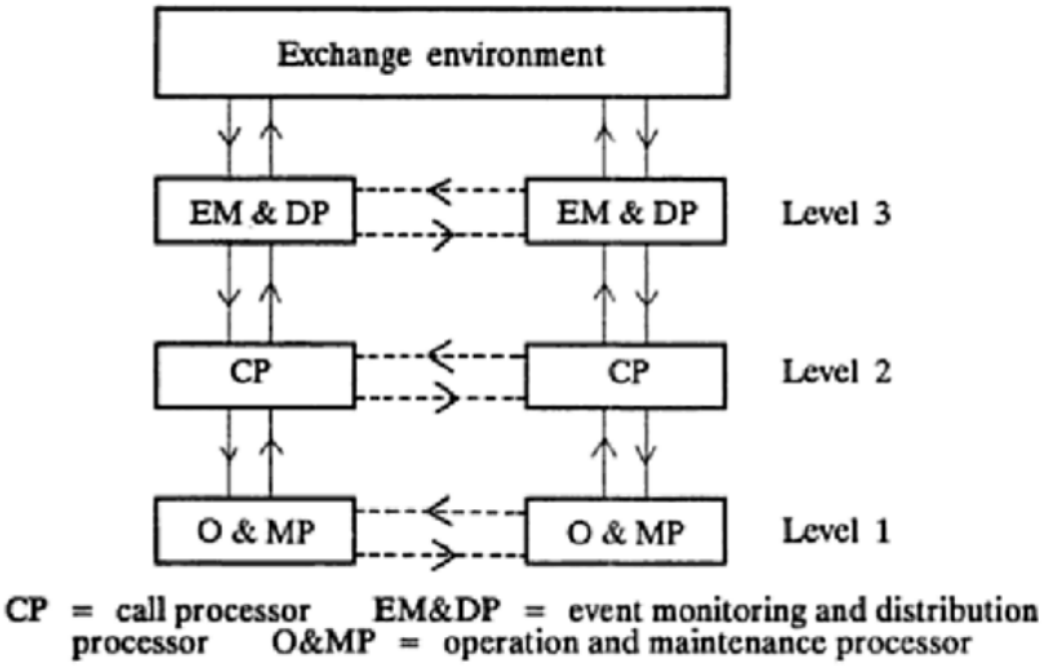


Fig. 3 (g): Dual chain distributed control [1]

- **Interrupt Processing:**before studying the Distributed SPC there is need to studyabout interrupt processing
- In Exchange, all the functions are classified into following categories:

  Event Monitoring and Distribution

  Call Processing

  Operation, Maintenance & Call Charging

- In exchange, the processor will process all the functions according to "Interrupt Processing"
- "Interrupt Processing" is done using the priority levels of the programs are being executed by the processor

✓ The following will interpret the concept of levels of processing or priority of the processing

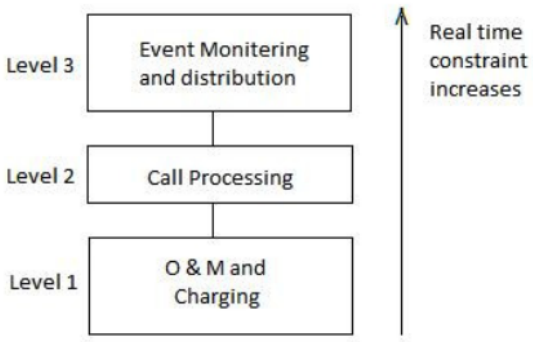


Fig. 4 (a): Interrupt processing [1]

- From the above diagram it is understood that
  - o Level 3 Process : Event Monitoring and Distribution
  - o Level2 Process : Call Processing
  - o Level 1 Process : Operation, Maintenance & Call Charging
  - o and the priority of Level 3 > Level 2 > Level 1
- Let a processor is currently executing a Level 1 Process like "Bill generation" of a consumer, meanwhile if exchange is assigned a new level 2 Process like "Call Connecting" then Processor will currently pause the Level 1 Process and will continue level 2 Process. After completing level 2 Process it will resume level 1 Process this depicts the "Interrupt Processing" as shown below:

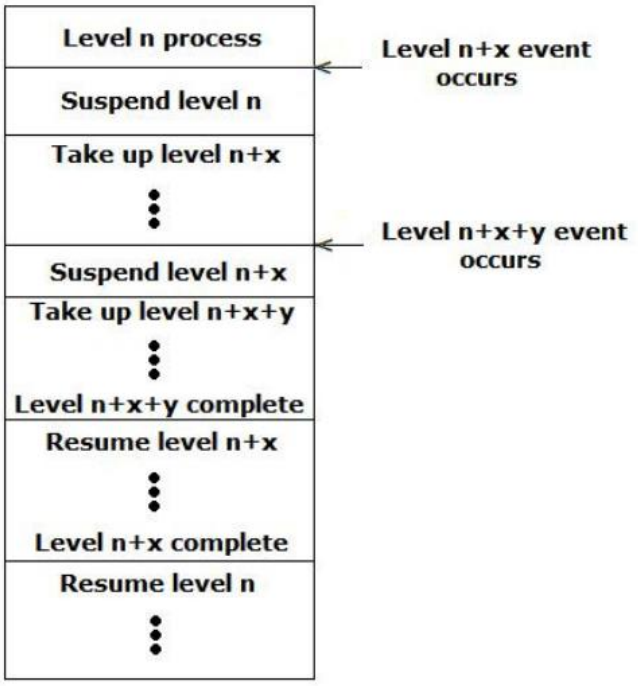


Fig. 4 (b): Interrupt processing priority [1]

Interrupts are basically in following types:

- o**Maskable Interrupt** : process instructions with different Priorities
- o **Non Maskable Interrupt**: The Highest Priority Interrupts like Power Failure,Reset Instruction

In interrupt processing when an interrupt occurs program execution is shifted to an appropriate service routine address in the memory through branch operation, this accomplishes with two methods:

Vectored Interrupt: In this method, the set of branch addresses are suppliedto the processor with different interrupting sources

Non Vectored Interrupt: In this method, the set of branch addresses aresupplied to the processor from fixed source

In case of Centralized SPC, only one processor is used to process all the exchange functions

where as in case of "Distributed SPC" three different processors are used for different levels of operations

Level 3 Processing

Level 3 Processing will include the functions like:

- Scanning
- Distribution
- Marking
- Controlling all incoming & Outgoing **local calls, STD Calls, ISD Calls, Fax &Data** services
- Control of all functions are carried by specially designed Processors with
- "Micro-programmed Control"

All levels of processing are depicted in the following figure:

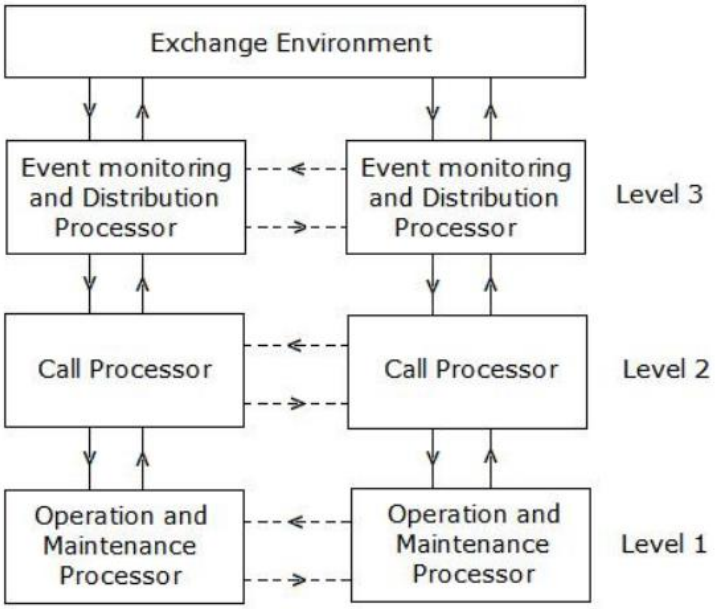


Fig. 4 (c): Level processing [1]

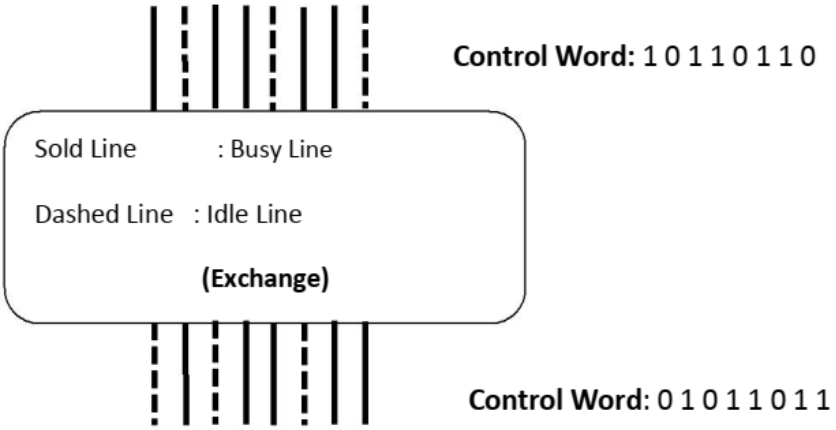
Here it is understood that, at each level of processing there are two set of processors are available one set is for active processing and another set is for standby

Coming back to Level 3 processing, here there is a keen difference between the classical "hard-wired control" and "Micro-programmed control"

Micro-programmed control	Hard-wired control
Flexible, Slower, More Expensive for small exchanges, easier to implement, complex programming, Introduction to new services & Easier to maintain	Non flexible, Faster, Less Expensive for small exchanges, Fixed Processing Speed, Difficult to Implement, Complex Functions, No scope of introducing new services, Difficult to maintain because of Electromechanical and lot of wires and connectors

Control Word: In case of Micro-Programmed Control, all the control functions arecontrolled by a Control Word which contains the status and control actions in the binary codes by which processor able to understands what operations to be performed by the exchange

For example an exchange contain number inlets and outlets in which some line are active and some lines are idle, in the following diagram indicates the status of lines and its binary codes in control word:



Level 2 Processing

Fig. 4 (d): Level 2 processing [1]

Level 2 Processing

- Level 2 Processing or Processor is also called Switching Processing or Switching Processor
- we the concept of "system availability" it is understood that, the availability of a telephone exchange for a user is completely depending upon the availability of Switching devices at the exchange to connect any two phones are computers. So switching unit play a major role in telephone exchange
- The architecture of switching processors is designed to for 99.9% availability and fault tolerance and security operations
- **Switching Occupancy:** The traffic handling capacity of the control equipment isusually limited by the capacity of the switching processor. The load on the switching processor is measured by its occupancy "t" estimated by the simple formula:

$$t = a + bN$$

- **t = Switching Processor capacity**
- **a = fixed overhead**
- **b = average time to process a call**
- **N = Number of calls per unit time**

Level 1 Processing

The Level 1 Processing includes a common general purpose computer to handle the

following operations:

- Bill Charging
- Bill distributing
  Monitor Traffic
- Fault tolerance
- Customer Support
- Making a new Service
- Disconnecting a requested serviceProcuring new Equipment
- Paying power bills of exchange.

This kind of operations is not required in a huge demand like Level 3 & Level 2 Operations Because of this reason, a central telephone exchange will provide service of Level 1 Processing. Meaning, all the nearby exchanges of a central exchange contain their own level 3 & Level 2 Processing units but Level 1Procesing unit is available at a central telephone exchange. In this way expenses of small exchanges are reduced

The below diagram will depict the concept of a central Operation and Maintenance and Call Charging Unit of some nearby exchange.

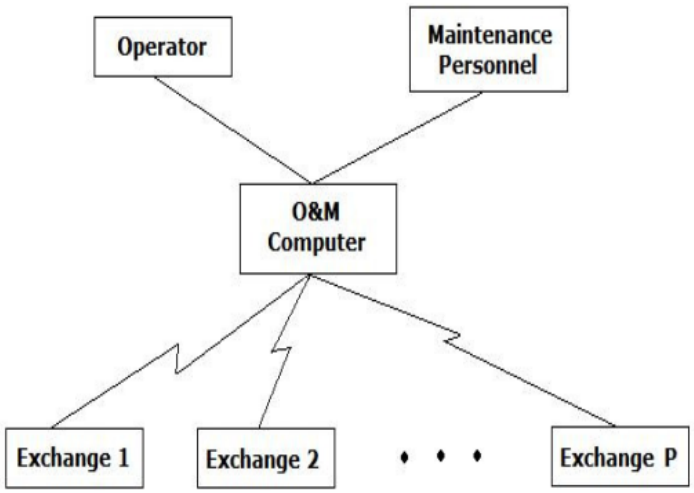


Fig. 4 (e): concept of a central Operation and Maintenance and Call Charging Unit [1]

Software Architecture

Software is basically two types:

i. System Software (Operating System)

ii. Application Software (Software based on Operating System)

Therefore a Special Design and Development is to be done for Switching Operating System
Process: an instruction executed by the processor is commonly called as a "Process"

Running Process: an instruction is currently executing by the processor

Ready Process: next instruction of running process and an instruction timed out isnormally called as a Ready Process

Blocked Process: a Process or instruction is said to be blocked when it is conditionallike "if", "while" because the execution of this instructions are depending on the results of the conditional statements. The below diagram will depict the state transitions between the "Running Process", "Ready Process" & "Blocked Process"

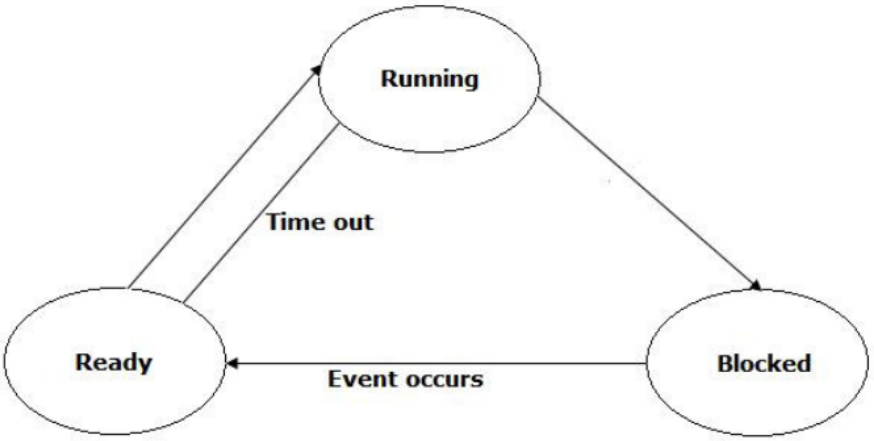


Fig. 4(f): Process States and Transitions [1]

Process Control Block: Each Control Process is represented by the operating systemby a "Process Control Block (PCB)" which is a data structure containing the following information about the process:

- Current State of the Process
- Process Priority and CPU Scheduling parameters
- Memory allocated to process
- Status of events and I/O resources associated with the process

✓ **Program Status Word:** which contains the address of the next instruction to be executed, the types of interrupts enabled or disabled currently

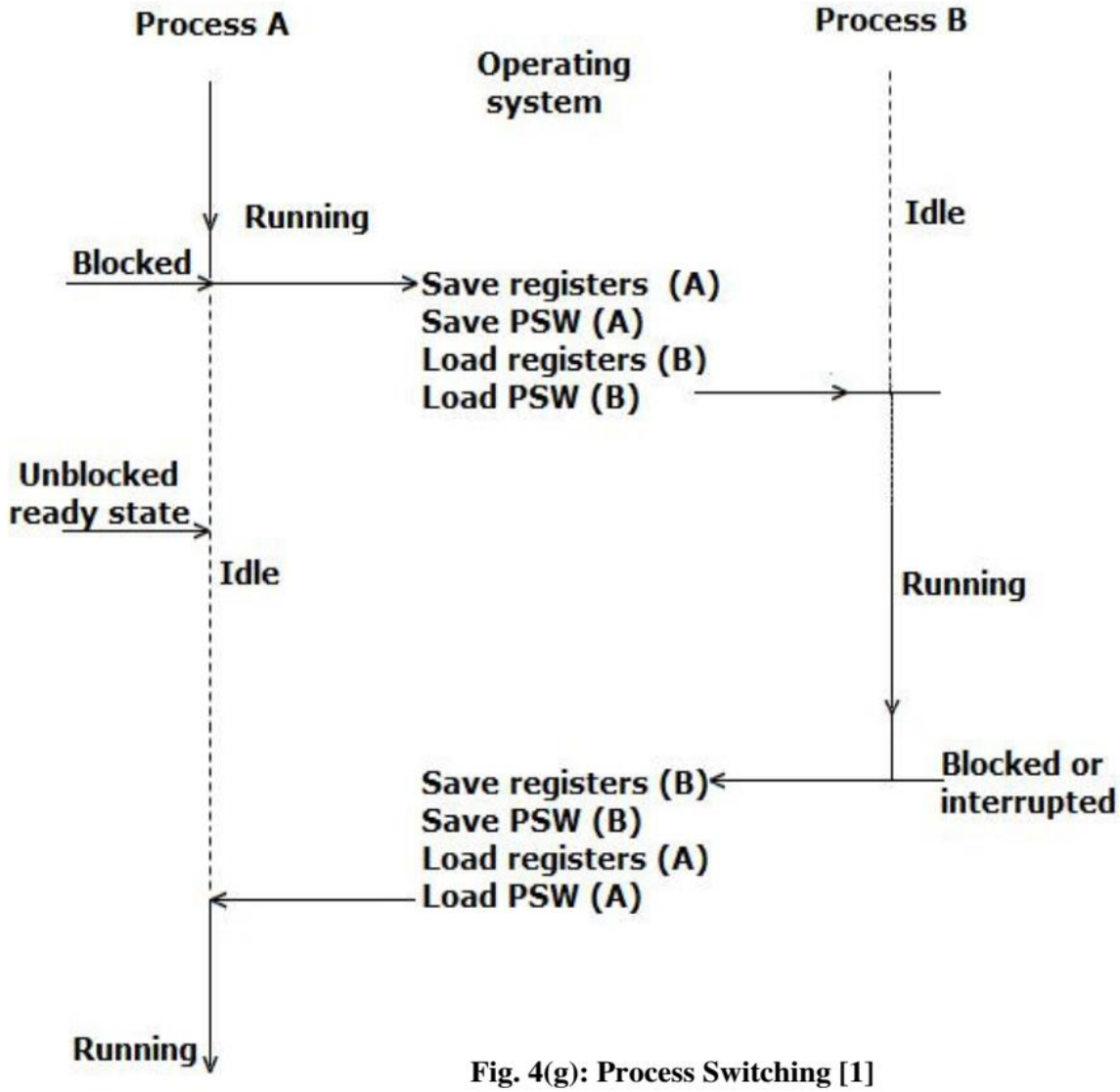


Fig. 4(g): Process Switching [1]

The above diagram depicts the process switching control of an operation system depending upon priority

Critical Region: when numbers of parallel processes are running by the operatingsystem, any time, any process may access common resources like memory space.

"When a process is accessing a common resource in any time of its execution, then the process is said to be in "Critical Region"

Semaphore: in order to avoid the problem of accessing any two or more processesare in critical state and to avoid "Deadlock" a variable "Semaphore" used

Semaphore contain a number (which is equal to the number processes of accessingthe common resources or be in critical state) by accessing this number operating system can manage between different processes in "Critical State" and by which, "Deadlock" is avoided.

SOFTWARE PRODUCTION

Basic factors associated with switching software

- Complexity and size of the software
- Long working life required
- Real time operation
- Stringent reliability and availability
- Software portability

Four stages in software production

- ✓ Functional specification
- ✓ Formal description and detailed specification
- ✓ Coding and verification
- ✓ †Testing and debugging

ENHANCED SERVICES

Categories of enhanced services

1. Services associated with the calling subscriber and designed to reduce the time spent on dialing and the number of dialing errors.

2. Services associated with the called subscriber and designed to increase the call completion rate.

3. Services involving more than two parties.

4. Miscellaneous services.

Category 1

Abbreviated dialing

Recorded number calls or no dialing calls.

Call back when free

Category 2

Call forwarding

Operator answer

Category 3

†Calling number record

†Call waiting

†Consultation hold

†Conference calls

Category 4

†Automatic alarm

†STD barring

†Malicious call tracing

STD : subscriber trunk dialing

TWO-STAGE NETWORKS

For any single stage network, there exists an equivalent multistage network.

Simple Two-stage NxN network

ANxN single stage network with a switching capacity of K connections can be realized by a two-stage network of NxK and KxN.

Fig. 5 (a): A two-stage representation of an NXN Network [1]

•First Stage: Any of the N inlets can be connected to any of the K outputs. NK switching elements.

•Second Stage: Any of the K input scan be connected to any of the N outlets. NK switching elements.

•There are K alternative paths for any inlet/outlet pair connection.

Simple Two-stage NxN network

Full connectivity/full availability

Any of the N inlets can be connected to any of the N outlets.

Example

Assume 10% of the subscribers to be active on average. Set K to be N/16. The number of switching elements is S=N2/8.

For N=1024, we have K=64, S=131072.

Note: Feasibility & Flexibility

Two-Stage Networks

Single stage vs. multistage networks

Inlet to outlet connection

Quality of link

Utility of cross-points

Establishment of a specific connection

Cross-point & path Redundancy

Number of cross-points

Capacitive loading problem

Blocking feature

Call establishing time

General two-stage networks

Terminology

Expanding network: M<N

Concentrating network: M>N

Square network: M=N

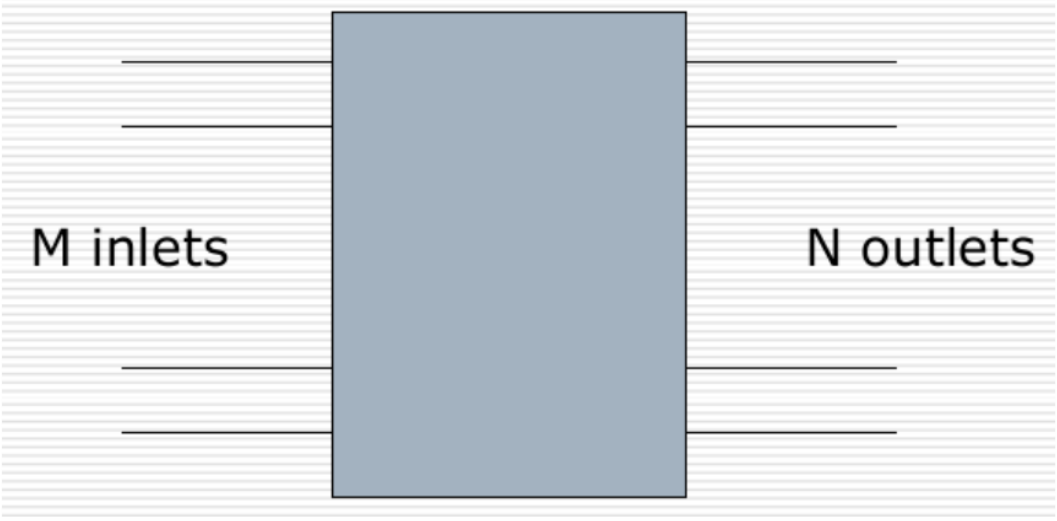


Fig. 5(b): General two-stage networks [1]

Architecture of General two-stage networks

Multiple small size matrices are used in each stage.

Easy to be realized in practice.

Flexible in system design.

NxN two-stage network design

Decomposition: M = p x r, N = q x s

Switching matrices: p x s and r x q

Full availability: There must be at least one out let from each block in the first stage terminatingas inlet on every block of the second stage.

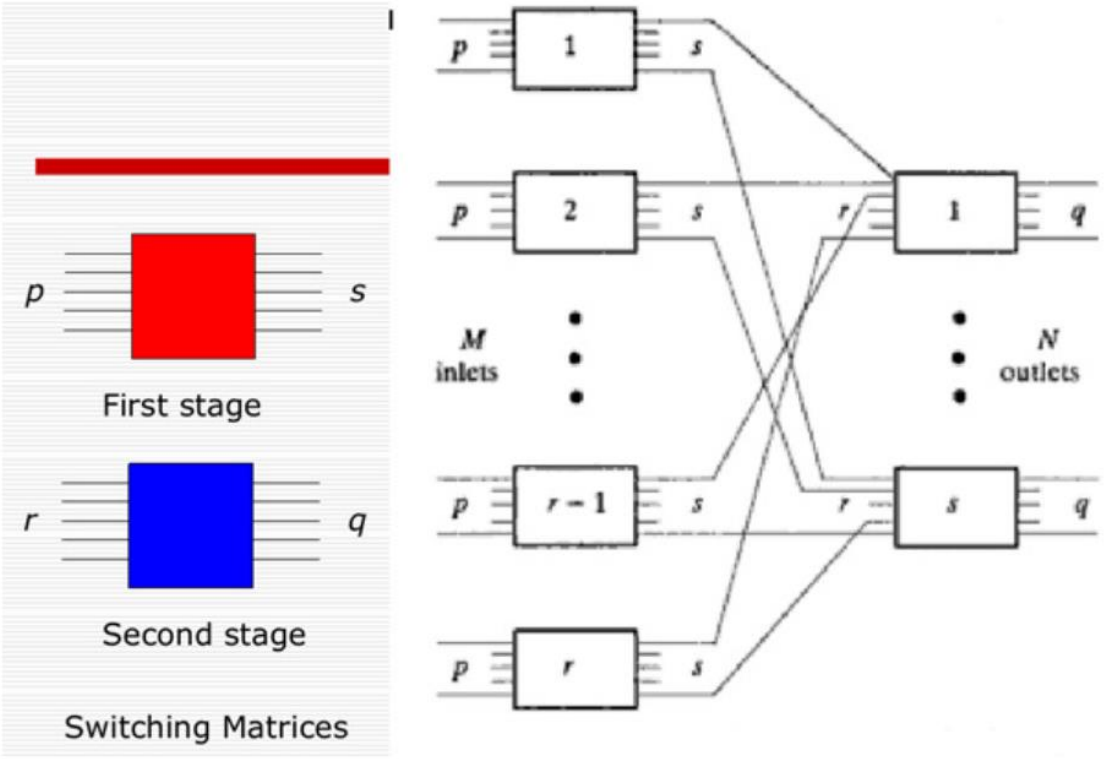


Fig. 5(c): General two-stage networks with multiple switching matrices. [1]

General two-stage networks

Parameters

Number of switching elements

S=psr+qrs=Ms+Nr

Switching Capacity i.e., the number of links between the first and the second stages.

SC=sr

General two-stage networks

Parameters

Blocking probability

Blocking condition 1

There are rxs calls in progress, and the (rs+1)-th call arrives;

The blocking probability PB is dependent on the traffic statistics.

Blocking condition 2

There is a call in progress from I-th block in the first stage to the J-th block in the second stage,and another call originating in the I-th block destined to the J-th block.

Blocking probability

$$P_B = \frac{M \propto (s-1)(\left(\frac{M}{r}\right)-1) \propto}{rs(s-1)}$$

General two-stage networks

†How to choose values of r and s?

„Both S and SC are proportional to r & s.

„Blocking probability PB is reversely proportional to r & s.

„Strategy: Tradeoffs should be made between cost and quality of service.

The values of r & s should be as small as possible but give sufficient links to provide a reasonable grade of service to subscribers.

Square two-stage networks

Baseline networks

Square switching matrices are used as building blocks.

p=r=s=q=N1/2

There are N1/2blocks, each block is a switching matrix of N1/2xN1/2 inlets and outlets.

Switching elements: S=2NxN1/2

Switching capacity: SC=N Support

Non-blocking networks

Why does blocking occur?

Only one link exists between a pair of first stage and second stage blocks.

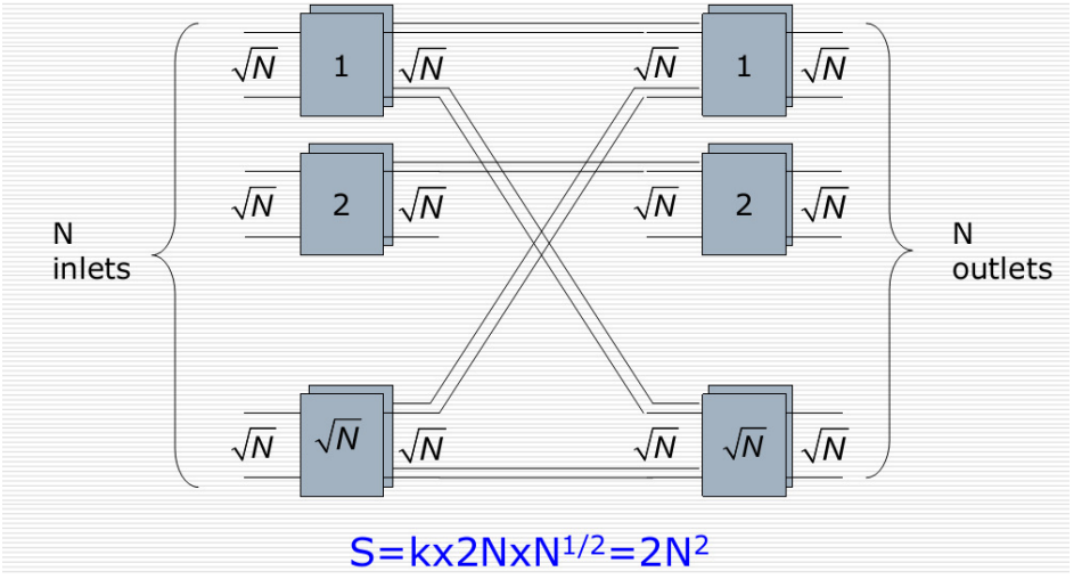
How to reduce the probability of blocking?

Provide more links between the first stage and second stage blocks.

„ How many links should be provided?

A group of k=N1/2links should be provided for each pair of first stage and second stage blocks. S=2N2.

In comparison with single stage network, the number of switching elements is doubled. N simultaneous calls only if the traffic is uniformly distributed.



Three-Stage networks

General structure of an NxN three-stage blocking network

Stage 1: p x s switching matrices

Stage 2: r x r switching matrices

Stage 3: s x p switching matrices

N=pxr, s is changeable

Compared with a two-stage network, there are s alternative pathsbetween apair of inlet and outlet.

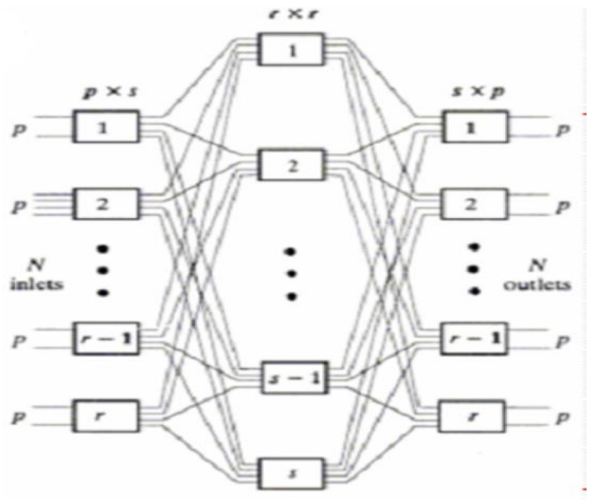


Fig. 5(d): General three-stage networks [1]

NxN three-stage blocking network

Number of switching elements

$$S=rps+sr2+spr=2Ns+sr2=s(2N+r2)$$

If square matrices are used in both the first and third stages, then p=s=N/r and S=2N2/r+Nr.

For a given value of N, there exists an optimal value of r which minimizes the value of S.

The optimal value of r is r= (2N) 1/2 and the corresponding minimum of S isSmin=2N (2N)1/2.

p=N/r=(N/2)1/2

NxN three-stage blocking network

Blocking probability analysis

Probability graph

Circle: stage

Line: link

A graph can be broken down into serial and parallel paths.

Notation

β: probability that a link is busy.

β'=1-β: probability that a link is free.

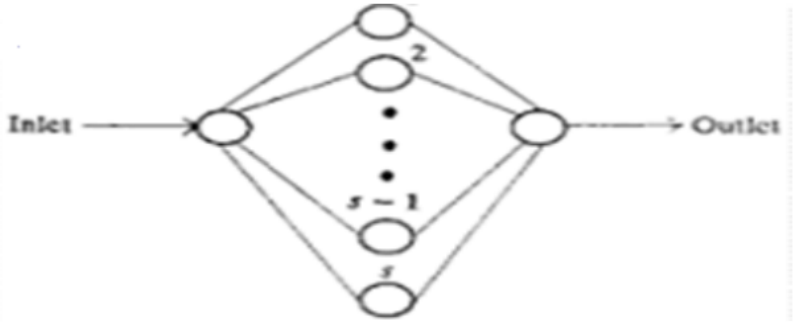


Fig. 5(e): Lee's graph for a three-stage network. [1]

Blocking probability analysis:

When s serial links complete a connection, the blocking probability is

$$PB=1-(1-\beta)^s$$

If there are s parallel links, the blocking probability is

$PB=\beta s$

Non-blocking three-stage networks

C. Clos: pioneer researcher of multistage non-blocking networks.

†Clos networks

- Multistage non-blocking and fully available networks.
- Much less switching elements are used than that in single stage networks.

Design strategy

Providing adequate number of blocks in middle stages. For three-stage networks, the value of s should be large enough.

Three-stage non-blocking configuration

Worst situation for blocking

p-1 inlets in a block I in the first stage are busy;

p-1 outlets in a block O in the third stage are busy;

The p-1 second-stage blocks, on which the p-1 outlets from block I are terminated on, are different from the p-1 second-stage blocks from which the links are established to the block O.

The free inlet of block I need to be terminated on the free outlet of block O.

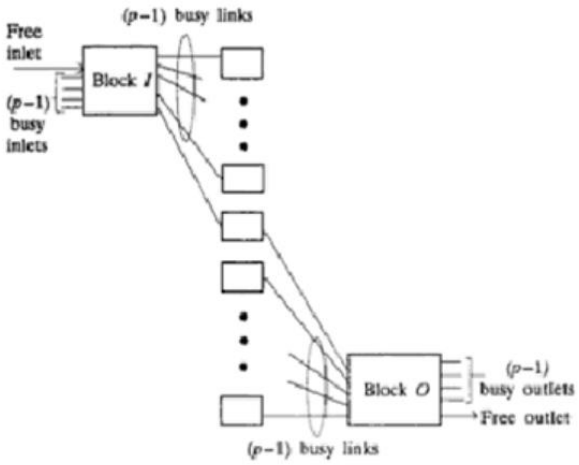


Fig.5 (f): Three-stage non-blocking configuration [1]

The number of blocks required in the second stage for non-blocking operation is

$s=2(p-1)+1=2p-1.$

The number of switching elements in the non-blocking configuration is given by

$$S=p(2p-1)r+(2p-1)r^2+p(2p-1)r$$
$$=2N(2N/r-1)+r^2(2N/r-1)$$
$$=(4N^2-2Nr)/r+2Nr-r^2$$

†

There exists an optimal value of r for minimizing the value of S.

Let dS/dr=0, we have $r^2(N-r)=2N^2$

For large values of N, we have N-r≈N.

Hence, $r=(2N)^{1/2}$, $p=N/r=(N/2)^{1/2}$

The minimum S is $S_{min}=4N(2N)^{1/2}$

Switching elements advantage ratio

$$\lambda = \frac{\text{S in nonblocking single-stage network, } N^2}{\text{S in nonblocking three-stage network, } 4N(2N)^{1/2}}$$

N-Stage networks

Further reduction in the number of switching elements is possible by using even higher number of stages than three.

Construction of multi-stage networks

By replacing the middle blocks with three-stage network blocks continually, any number of stages can be obtained.

Construction of five-stage ~

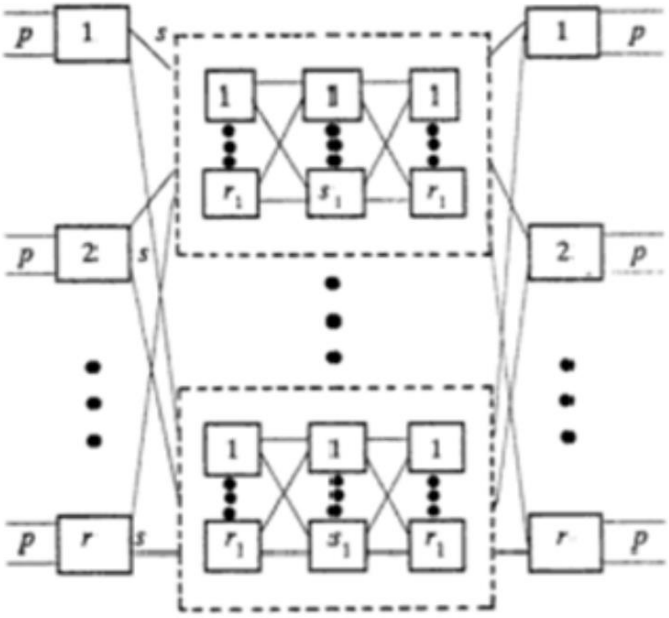


Fig.5 (g):Five-stage switching network [1]

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