Telecommunication Switching:

Various facilities of digital switching and transmission are the reason why the analog switching is slowly getting replaced by digital switching. The incorporation of digital switching and transmission technique into telecommunications altered the whole telecommunication industries setup. The reliability of digital switching system is becoming increasingly important for users of telephone services. Voice and/or data can be represented using digital signals efficiently than analog signals.

A switching system is called digital when the input to and output from the switching system can directly support digital signal. Many basic elements of the digital switching system and its operation are very similar to the stored program control (SPC) switching system. The cost of an analogue switch is roughly proportional to the number of cross points, but the cost relationship in digital switching is different.

The functions of the digital switching network are to connect pairs of channels. So that information arriving at the switching centre in a particular channel on one PCM multiplex system can be passed to some other channel on an outgoing PCM multiplex systems. To achieve this switching, two processes referred to as time switching and space switching are used. The principles of these two switching process are described in this chapter.

In digital data communication (analog or digital signal), a fundamental requirement is that the receiver should know the starting time and duration of each bit that it receives. To meet this requirement a synchronous and synchronous transmission are used. These two transmission techniques are described in this chapter.

Evolution of Digital Switching System:

The early version of electronic switching system is the stored program control (SPC). The SPC systems have temporary memory for storing transient call information and to carry programming information. The SPC performs line control, trunk control, ancillary control, maintenance control etc. The instructions required for performing these operations are resided in a single processor. For reliability or high availability, the processor may be duplicated. Thus SPC uses centralized software and hardware architectures.

A modern digital switching system employs a number of processors not uses distributed software and hardware architectures. The digital switching system also referred as Electronic Switching System–III generation is purely electronic in operation, the switching process is by time division/digital transmission, the type of control is stored program common control and the network uses pulse code modulation.

TIME DIVISION SWITCHING

Time division switching involves the sharing of cross points for shorter periods of time. This paves way for the reassign of cross points and its associated circuits for other needed connections. Therefore, in time division switching, greater savings in cross points can be achieved. Hence, by using dynamic control mechanisms, a switching element can be assigned to many inlet-outlet pairs for few microseconds. This is the principle of time division switching. Time division switching uses time division multiplexing to achieve switching. Two popular methods that are used in time division multiplexing are (*a*) the time slot interchange (TSI) and (*b*) the TDM bus. In ordinary time division multiplexing, the data reaches the output in the same order as they sent. But TSI changes the ordering of slots based on the desired connections. The de-multiplexer separates the slots and passes them to the proper outputs. The TDM uses a control unit. The control unit opens and closes the gates according to the switching need. The principle of time division switching can be equally applied to analog and digital signals. For interfacing sampled analog signals but not digitized, the analog time division switches are attractive. But for larger switches, there are some limitations due to noise, distortion and crosstalk which normally occurs in PAM signals. Thus analog switching is now used only in smaller switching systems. In this section, the analog time division switching and digital time division switching are described briefly.

Analog Time Division Switching

Fig. 6 shows a simple analog time division switching structure. The speech is carried as PAM analog samples or PCM digital samples, occurring at 125 μs intervals. When PAM samples are switched in a time division manner, the switching is known as analog time division switching. If PCM binary samples are switched, then the switching is known as digital time division switching. A single switching bus supports a multiple number of connections by interleaving PAM samples from receive line interfaces to transmit line interfaces. There are two cyclic control stores. The first control store controls gating of inputs onto the bus one sample at a time. The second control store operates in synchronism with the first and selects the appropriate output line for each input sample.

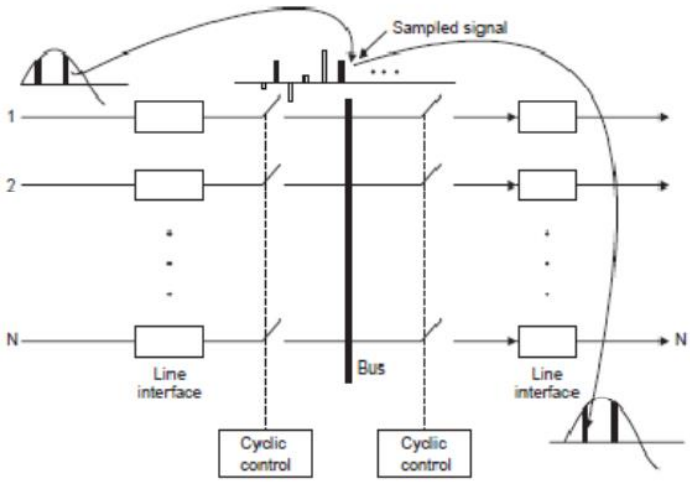

Figure 6: Analog time division switching [1]

The selection of inlet/outlet is controlled by various ways. The (a) cyclic control and (b) memory based control are the important controls and described in the following paragraphs.

Cyclic control: The cyclic control is organized by using Modulo-N counter and k to 2k decoder as shown in Fig. 7.

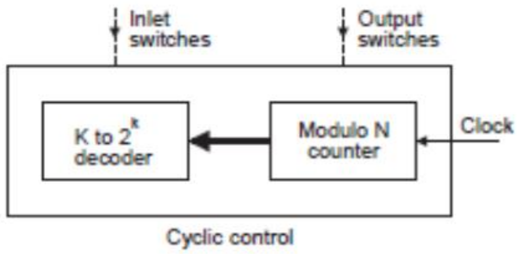

Figure 7: The cyclic control [1]

The k and N are related by $\lceil \log_2 N \rceil = k$

where N = number of inlets/outlets

k = decoder size.

$\lceil\ \rceil$ = gives the lowest integer. It means k may be assumed lowest integer or more than that.

This kind of switching is non-blocking but lack of full availability as it is not possible to connect inlet to any outlet. The switching capacity or number of channel supported by cyclic controlled system is

$$C = \frac{125\,\mu\text{sec}}{t_s}$$

The numerator 125 μsindicates the time taken to scan inlet and outlet and the denominator t_s is the time in μs to setup connection. Memory based control. Full availability can be achieved if any one control is made memory based. If the input side is cyclically switched and the outlets are connected based on the addresses of the outlets stored in contiguous location is referred as input controlled or input driven. If the outlets are cyclically switched, the switch is referred as output controlled or output driven. As the physical connection is established between the inlet and the outlet through the common bus for the duration of one sample transfer, the switching technique is known as time division space multiplexing. For this system,

$$C = \frac{125\,\mu\text{sec}}{t_i + t_m + t_d + t_t}$$

Where,t_m = time to read the control memory

t_d= time to decode address and select the inlet and outlet.

t_i= time to increment the modulo N counter.

t_t= time to transfer the sample.

The capacity equations are valid only for an 8 kHz sampling and non-folded network (can be used for folded network with certain changes in network). The switching Capacity in the memory controlled is equal to N. The use of cyclic control in input or output controlled switches restricts the number of subscribers on the system rather than the switching capacity since all the lines are scanned whether it is active or not. No restrictions on subscriber number and full availability of the switching system can be achieved by designing a switching configuration with control memory for controlling both inlets and outlets. This configuration referred to as memory controlled time division space switch is shown in Fig. 8. As each word of the control memory has inlet address and an outlet address, the control memory width is 2 $\log_2$ N. The control memory words are readout one after another. Modulo counter is updated at the clock rate. For the path setup of kth inlet and jth outlet, the addresses are entered in control memory and path is made. Then the location is marked busy. When conversation is terminated, the addresses are replaced by null values and location is marked free. Hence

$$C = \frac{125}{t_s}\ \mu\,\text{sec, where } t_s = t_i + t_m + t_d + t_t$$

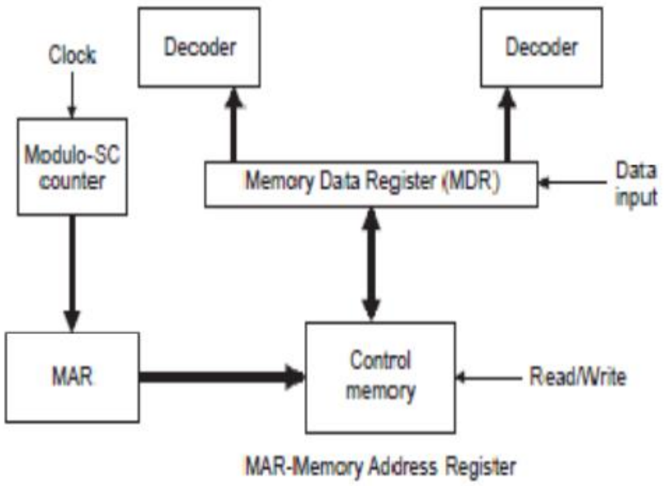

Figure 8: Memory controlled time division space switch [1]

The switching matrix described above is referred to as time multiplexed switching as the switch in this configuration is replicated once for each time slot.

Digital Time Division Switching

The analog time division switching is useful for both analog and digital signals. The digital time division multiplexed signals usually requires switching between time slots as well as between physical lines. The switching between time slots is usually referred as time switching. Similar to analog time division switching the switching structure can be organized expect the use of memory block in place of the bus. This adds the serial to parallel and parallel to serial bit conversion circuitry's as the input to the memory block should be in parallel form. The time division switch can be controlled in any of the following three ways.

Basic operation: The basic requirement of time division switching is that the transfer of information arriving at in a time slot of one input link to other time slot of any one of output link.

A complete set of pulses, arriving at each active input line is referred to as a frame. The frame rate is equal to the sample rate of each line. A time switch operates by writing data into and reading data out of a single memory. In the process the information in selected time slots is interchanged as shown in Fig. 9.

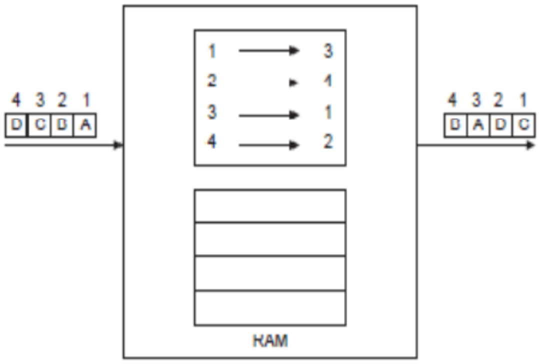

Figure 9: Time division switch[1]

In TSI operation, inputs are sequentially controlled and outputs are selectively controlled. The RAM has several memory locations, each size is the same as of single time slot. Fig. 10 shows the general arrangement of the time division time switching.

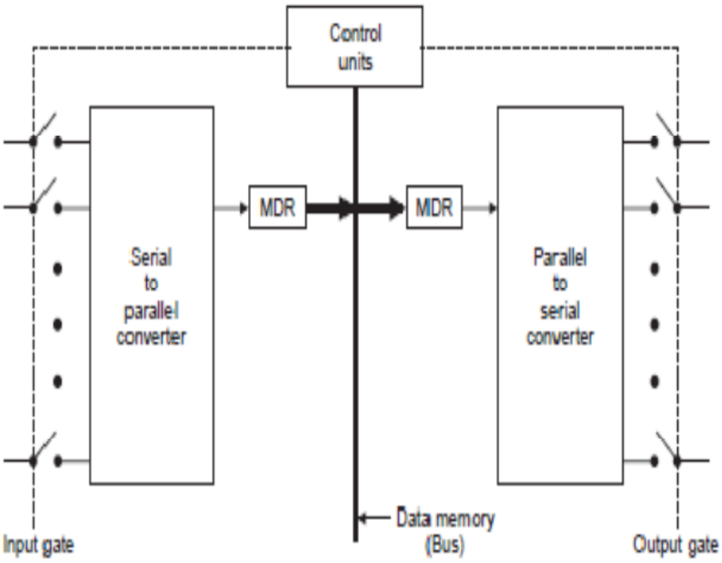

Figure 10: General arrangement of time division switching [1]

The serial to parallel and parallel to serial converter are used to write the data into the memory and read the data out of memory. For convenience, two MDR are shown, but MDR is a single register. Gating mechanism is used to connect the inlet/outlet to MDR. The input and output lines are connected to a high speed bus through input and output gates. Each input gate is closed during one of the four time slots. During the same time slot, only one output gate closed. This pair of gates allows a burst of data to be transferred from one input line to a specific output line through the bus. The control unit opens and closes the gates according to switching need. The time division time switch may be controlled by sequential write/random read or random write/ sequential read. Fig. 10 depicts both modes of operation and indicateshow the memories are accessed to translate information from time slot 2 to time slot 16. Both methods use a cyclic control.

Fig. 10 (a) implies that specific memory locations are dedicated to respective channels of the incoming TDM link. Data are stored in sequential locations in memory by incrementing modulo N counter with every time slot. Thus incoming data during time slot 2 is stored in the second location within the memory. On output, information retrieved from the control store specifies which address is to be accessed for that particular time slot. Thus sixteenth word of control store contains the number 2, implying that the contents of data store address 2 is transferred to the output link during outgoing slot 16. Random write/sequential read mode of operation is opposite to that of sequential write/ random read. Incoming data are written into the memory locations as specified by the control store, but outgoing data are retrieved sequentially under control of an outgoing time slot counter. The data received during time slot 2 is written directly into data store address 16 and it is retrieved during outgoing TDM channel number 16.

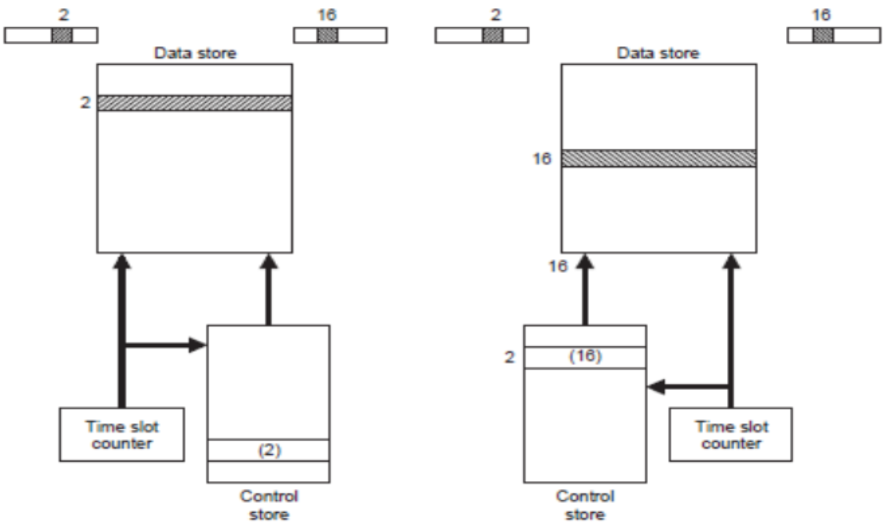

Figure 10 (a) : Memory locations allocated to TDM [1]

TWO DIMENSIONAL DIGITAL SWITCHING

Combination of the time and space switches leads to a configuration that achieved both time slot interchange and sample switching across trunks. These structures also permit a large number of simultaneous connections to be supported for a given technology. Large digital switches require switching operations in both a space dimension and a time dimension. There are a large variety of network configurations that can be used to accomplish these requirements. The incoming and outgoing PCM highways are spatially separate. So the connection of one line of local exchange obviously requires space switching to connect to the channel of outgoing highways. Thus the switching network must be able to receive PCM samples from one time slot and retransmit them in a different time-slot. This is known as time slot interchange, or simply as time switching. Thus the switching network must perform both space and time switching.

The space switching and time switching may be accomplished in many ways. A two stage combination switch may be organized with time switch as first stage and the space switch as the second stage or vice versa. The resulting configurations are referred as time space (TS) or space time (ST) switches respectively. Three stage time and space combinations of TST and STS configurations are more popular and flexible. Very large division switches includes many combinations of time and space switches. Typical configurations are TSST, TSSSST, and TSTSTSTS. These switches support 40000 lines or more economically. The general block diagram involving time and space switching is shown in Fig. 11.

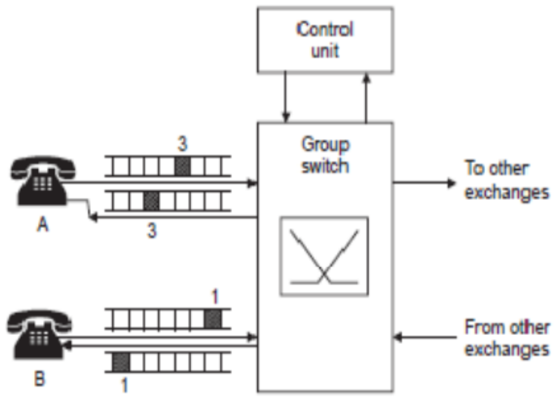

Figure 11: Time and space switching [1]

The main task of the switching part is to interconnect an incoming time slot and an outgoing time slot. The unit responsible for this function is group switch. There are two types of building block in the digital group switch. They are time switch and space switch. In Fig. 7, the subscriber makes a local call to B. The control unit has assigned time slot 3 to the call on its way into the group switch, and time slot 1 on its way out of the group switch (to B). This is maintained during the entire call. Similarly B to A also carried out. The fundamental design and structure of the two switches viz. time switch and space switch are described in the following sections.

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