Space and Time Switches

Space switch: Fig. 12 shows a typical space switch. It uses a space array to provide switching generally the space switch consists of a matrix of M × N switching points where M is number of inlets and N is number of outlets. A connection between an inlet and an outlet is made by the simple logic gates (AND gates). As logic gates are unidirectional, two paths through switching matrix must be established to accommodate a two way conversation. The logic gate array can serve for concentration, expansion or distribution depending on M is larger, smaller or equal to N. Fig. 8 shows only one voice direction. However, the corresponding components are available for the opposite direction too. A number of M, of X slot multiplexers, provide the inputs and the outlets are connected to N, X slot de-multiplexers. The gate select memory has X locations. The word containing information about which cross point is to be enabled is decoded by the translator. During each internal time slot, one cross point is activated. In the shift to the next interval time slot, the control memory is incremented by one step, and a new cross point pattern is formed in the matrix.

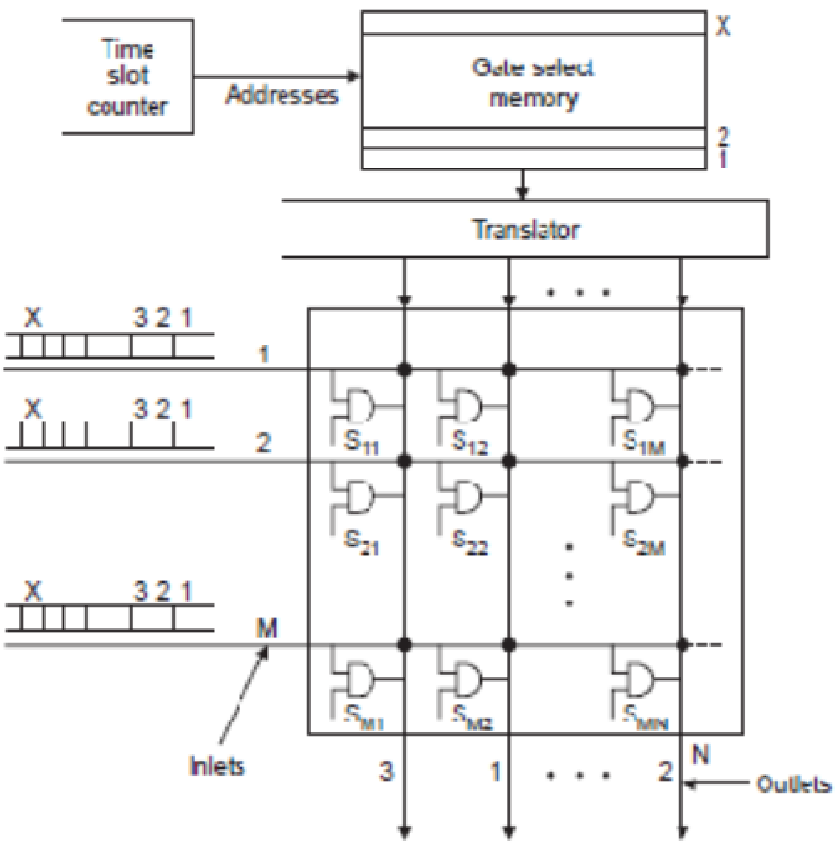

Figure 12: Space switch [1]

Time switch: The time-slot interchange (TSI) system is referred to as time switching (T-switching). Fig. 13 shows the block diagram of time switch.

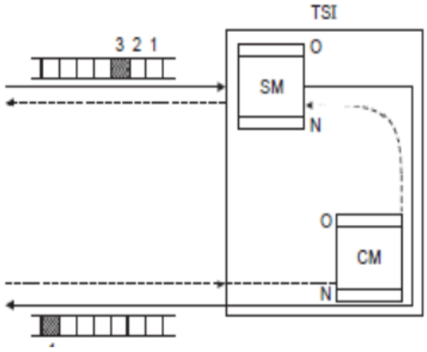

Figure 13: Time switch [1]

Each incoming time slot is stored in sequence in a speech memory (SM). The control memory (CM) determines in which order the time slots are to be read from SM. This means that a voice sample may be moved from say incoming time slot 3 to outgoing time slot 1.

Time-space (TS) Switching: This switch consists of only two stages. This structure contains a time stage T followed by a space stage S as shown in Fig. 14. Thus this structure is referred to as time-space (TS) switch. The space arrays have N inlets and N outlets. For each inlet line, a time slot interchangerwith T slots is introduced. Each TSI is provided with a time slot memories (not shown). Similarly a gate select memory needs to be provided for the space array (not shown).

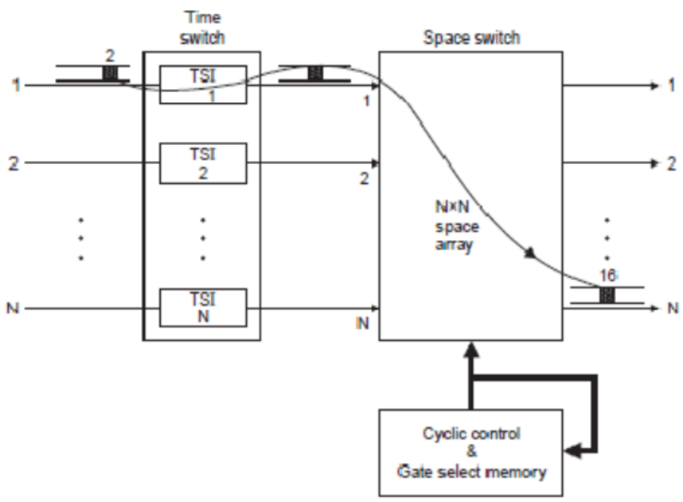

Figure 14: Time space switching [1]

The transmission of signals carried out from sender to receiver through multiplexer input and demultiplexer output. The reverse communication is also similar. Thus a hybrid arrangement is needed to isolate the transmitted signal from the received signal. The basic function of the time switch is to delay information in arriving time slots until the desired output time slot occurs.

Let the communication is to take place between subscriber A and B. Let A is assigned time slot 2 and line 7 and subscriber B is assigned time slot 16 and line 11. Then the signal moved from time slot 2 to time slot 16 by the time-slot exchanger and is transferred from line 7 to line 11 in the space array. Similarly, the signal originated by B is moved from slot 16 to slot 2 through line 11 to 8. The cyclic control and gate select memory contains the information needed to specify the space stage configuration for each individual time slot of a frame. The time stage has to provide decays ranging from one time slot to a full frame. During each outgoing time slot, control information is accessed that specifies inter stage link number to output link. During other time slots, the space switch is completely reconfigured to support other connections.

Let each time slot interchanger have T slots. If the space array is a N × N, then the simultaneous connections possible is NT. If T = 128 and N = 16, 2048 connections can be supported. This structure is not free of blocking. The control store is a parallel end around shift resister. If space array is at the inlet side and time switch is at the output side, the structure is referred as space time (ST) switching. Both TS and ST arrangements are equally effective. TS system is used in DMS 100 digital switching system developed in Canada (1979). It handles 61000 trunks and accommodates 39000 trunks.

Blocking probability :

The blocking probability of TS switching is calculated as follows.

The probability that a subscriber A is active $= \frac{\rho}{T}$ ...(5.28)

where ρ = fraction of time that a particular link is busy measured in Erlangs

T = number of time slots in a frame.

The probability that any other subscriber is active on the same link

$$= \frac{(T-1)\rho}{T} \qquad ...(5.29)$$

The probability that a particular called subscriber is chosen by A

$$= \frac{1}{NT} \times \frac{1}{T} \qquad ...(5.30)$$

where N = Number of inlets (or outlets) for N × N space array.

NT = Simultaneous connection ...(5.31)

The probability that the same time slot on a different outlet is chosen by the other subscribers on the same inlet

$$= \frac{(T-1)(N-1)\rho}{T(NT-1)} \quad \text{...(5.32)}$$

From Blocking probability $= B = \left(\frac{\rho}{T \times NT}\right)\left(\frac{(T-1)(N-1)}{T(NT-1)}\right)$

As T >> 1 and N >> 1, & NT >> 1

$$B = \frac{P}{NT^3} \quad \text{...(5.33)}$$

The TS switch can be made non-blocking by using an expanding time switch (T to T^2 slots) and a concentrating space switch (which is complex).

The number of cross points in space stage can be easily calculated which is based on the array size. The time stage uses significant amount of memory which adds the cost of the whole system. To take this into account the cost of memory bit is assumed one hundredth of the cost of cross point. Thus,

$$\text{Implementation complexity} = N_X + \frac{N_B}{100}$$

where N_X = Number of space stage cross points

N_B = Number of bits of memory.

The N_B not only includes the time stage memory arrays, but also the control memory (store) of the time stage and space stage. Thus,

$$N_B = N_{BX} + N_{BT} \quad \text{...(5.35)}$$

where N_{BX} = Number of memory bits for the space stage control store

= N × (Number of control words) (number of bits per control word)

N_{BT} = Number of memory bits in the time stage equal to sum of time slot interchange and the control store bits.

= N × number of channels × number of bits per channel + N × number of control words × number of bits per control world.

Example 5.3. If N = 80, N_{BX} = 13, 440 and N_{BT} = 24,960 for a typical TS switch, calculate the implementation complexity.

$$IC = N_X + \frac{N_{BX} + N_{BT}}{100} = 80 \times 80 + \frac{13440 + 24960}{100}$$

IC = 6784 equivalent cross points.

As the number of cross points in space array is equal to 6400, the total cost is dominated by the space stage.

STS and TST Switching:

The TS structure is of blocking nature. Let A and B are the subscribers using different time slot on the same line want to connect to two subscribers C and D using same time slot on different lines. A and B can be moved to the same time slot but during that time slot, the inlet line can be connected to C's line or D's line but not both. This is the significant limitation of the structure. Moreover, time stage switching is generally less expensive than space stage switching as digital memory is much cheaper than digital cross points (AND gates). The multiple stages overcome the limitations of the individual switches and cost savings can also be achieved. TST, STS, TSST, TSSSST and TSTSTSTSTSTSTS are the switching system configurations used in digital switching system. However, the TST structure is the most common.

STS Switching:

In STS switching, the time stage is sandwiched between two space arrays. The digital switching system ITS 4/5 of USA (1976) uses the STS switching configuration. It handles 3000 trunks and accommodates 1500 Erlangs of traffic. Fig. 15 shows the space-time- space (S-T-S) switching network for M incoming and outgoing PCM highways. Establishing a path through an STS switch requires finding a time switch array with an available unit's access during the incoming time slot and an available read access during the desired outgoing time slot. The input side space stage as well as the output side space stage is free to utilize any free time switch modules. In the diagram shown in Fig. 11, the time slot 2 is connected to the TSM 2 where the time slot allotted is 16 and passed to the $(M - 1)^{th}$ line of output space array. Thus the path is provided. This structure is of non-blocking nature.

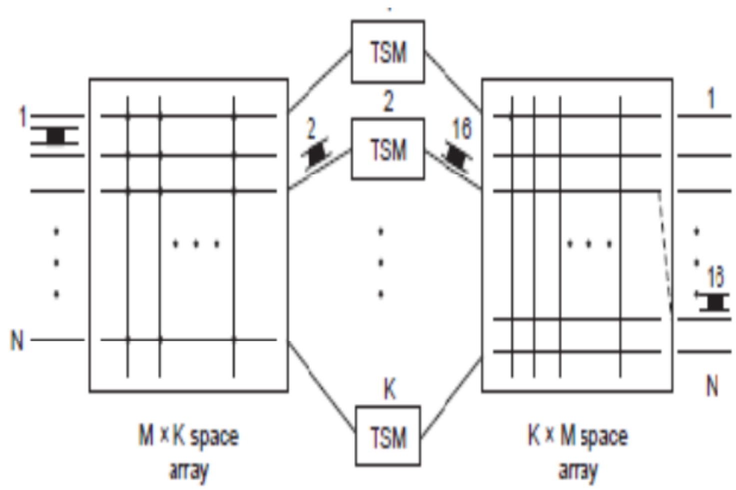

Figure 15: STS Switching[1]

Blocking probability: The STS switch is identical to the probability graph of three stage space switches. Similar to that, the blocking probability of an STS switch is

$$B = \left[1 - \left(1 - \frac{p}{\beta}\right)^2\right]^K$$

Where p = probability that a link is busy

N = is the factor by which the percentage of links that are busy is reduced. ($\beta < 1$)

K = number of center stage TSM.

Implementation capacity (IC):

While calculating IC, the total number of two space stage cross points, total number of two space stage control bits, number of time stage memory bits and number of time stage control bits are to be considered. Thus,

$$IC = 2KN + \frac{2KC \log_2 N + KC(8) + KC \log_2 C}{100}$$

Where K = Minimum number of center stage TSM to provide desired grade of service

C = number of channel.

TST Switching:

In TST switching the space stage is sandwiched between two time stage switches. Of all the multistage switching, TST is a popular one. Popular digital switching systems using TST are tabulated in table 2.

Some important features of TST switches are:

(i) Low blocking probability. An incoming channel time slot may be connected to an outgoing channel time slot using any possible space array time slot. Thus there are many alternative paths between two subscribers. This concept reduces the blocking probability of a three stage combination switch.

(ii) Stage independency. The space stage operates in a time-divided fashion, independently of the external TDM links. The number of space stage time slots L does not coincide with the number of external TDM time slots T.

Type	Characteristics	
	Max. no. of trunks	Traffic (Erlangs)
E 10 B (France, 1970)	3600	1600
AXE 10 (Sweden 1978)	65000	30000
EWSD (Germany 1980)	60000	30000
CTD SEAX (USA, 1982)	49000	36000
C-DOT MAX-XL (India)	40000	47000

Table 2: Digital switching systems using TST and its characteristics [1]

(iii) Implementation advantage. The factors to be considered for switching design and implementation are traffic loads, modularity, testability, expandability and simple control requirements. For large switches with heavy traffic loads, the TST have good implementation advantage.

(iv) More cost effective. If the input channel loading is high, the time expansion of TST and space expansion of STS are required. Time expansion of TST can be achieved at less cost than space expansion of STS. In comparison with STS, the TST have certain limitations. For small switches, the STS architectures are less complex to implement than TST. The control requirements of STS are simpler than TST.The principle of operation of TST switching is shown in Fig. 16. In figure, two flows of time slots, one for each direction are connected together.

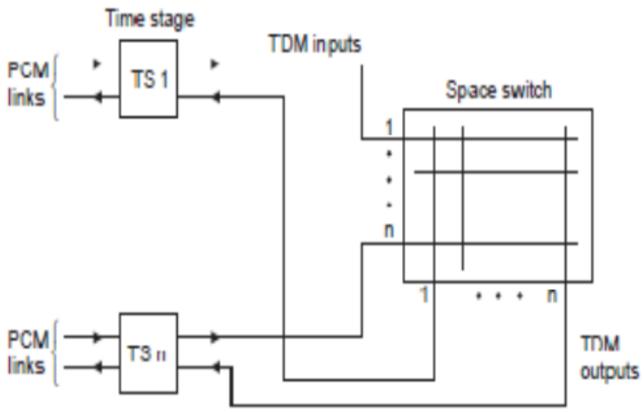

Figure 16: Principle of TST switching [1]

The functional block diagram which explains the transfer of signals from inlet to outlet is shown in Fig. 17. The information arriving at the incoming link of TDM channel is delayed in the· inlet times stage until an appropriate path through the space stage is available. Then the information is transferred through the space stage to the appropriate outlet time stage. Here the information is held until the desired outgoing time slot occurs. Any space stage time slot can be used to establish a connection. The space stage operates in a time divided fashion, which isIndependent of the external TDM links. There are many alternative paths between a prescribed input and output unlike a two stage network which has only one fixed path.

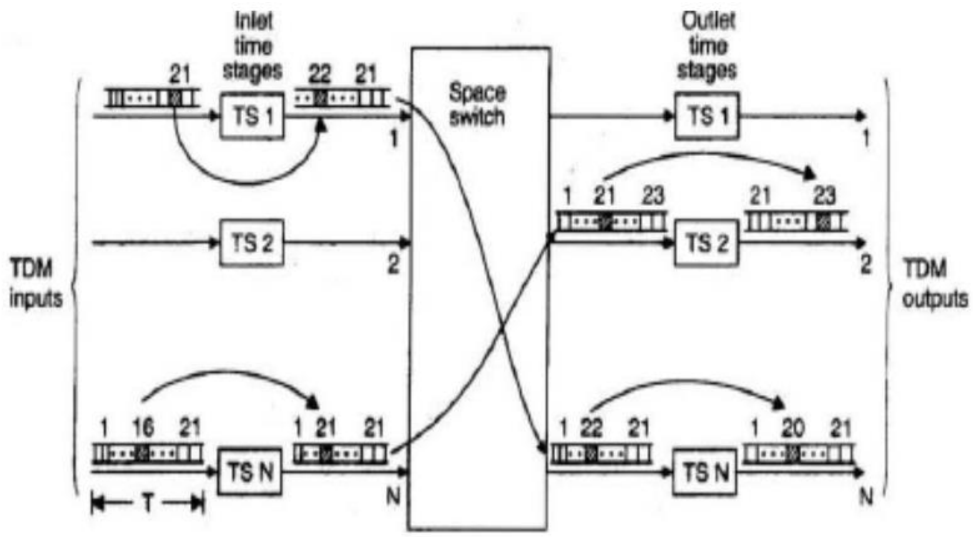

Figure 17: TST switching structure [1]

Blocking probability: The blocking probability is minimized if the number of space stage time slots L is made to be large. By direct analogy of three stage space switches, the TST switch is strictly non-blocking if

L = 2T - 1

Where T = number of time slot of time switch.

L = number of space slot of space switch.

The probability graph of TST switch with non-blocking stage is shown in Fig. 18.

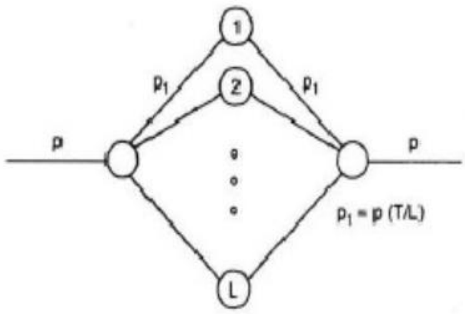

Figure 18: Probability graph[1]

The general expression of blocking probability for a TST switch with non-blocking individual stage is

$$B = [1 - (1 - pT/L)^{n}]^{L}$$

For 3 stage $$B = [1 - (1 - \rho(T/2))^{2}]^{2}$$

Implementation complexity:

The implementation complexity (IC) of a TST switch can be derived as

$$IC = N^2 + \frac{NL\log_2 N + 2NT(8) + 2NL\log_2 T}{100}$$

Where N=No. of TDM links

T= No. of channel

L= No. of Time slot of space switch

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